

portions of the gate 147 that are buried in the substrate are isolated by the sidewall/dielectric 145, but are spaced from and do not extend into the source and drain regions. This is apparently reflected in the Office Action's lack of citation to any reference in connection with the asserted teachings of "the source and drain implantations extending along part of the side walls of the trench" at page 3. Moreover, the Office Action has erroneously alleged that regions 143n and 144n are "shallow contact regions," where these regions are the actual source and drain regions themselves (*see, e.g.*, column 15:3-12), with contacts 148 and 149 being formed on the upper surface of the substrate. Of note, the further cited regions 171n and 161n are respectively n-type offset regions (*see, e.g.*, column 16:11-21).

The '231 reference thus has no bearing upon the claimed invention and limitations directed to a gate trench with sidewalls and endwalls extending into and insulated from source/drain regions and their respective contact regions. Applicant notes that this is consistent with claim 1, as well as new claims 11 and 12, which further characterize the trench (*e.g.*, as being located within and surrounded on ends and sides by source/drain regions). This is exemplified, for example, by the dashed lines in the cross-section shown in FIG. 2, as further consistent with the top view shown in FIG. 3 from the instant application, both of which are copied below for convenience.

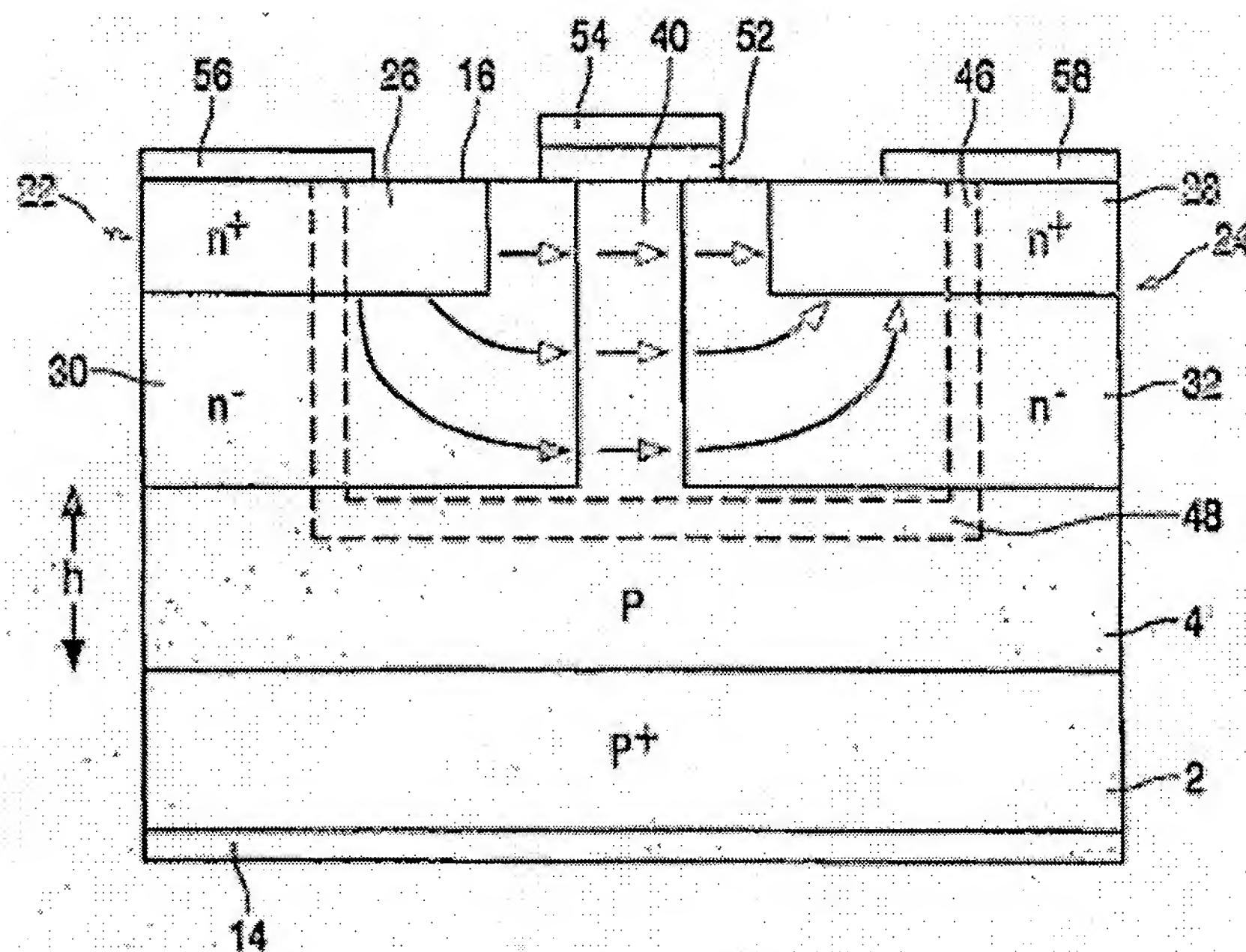


FIG. 2

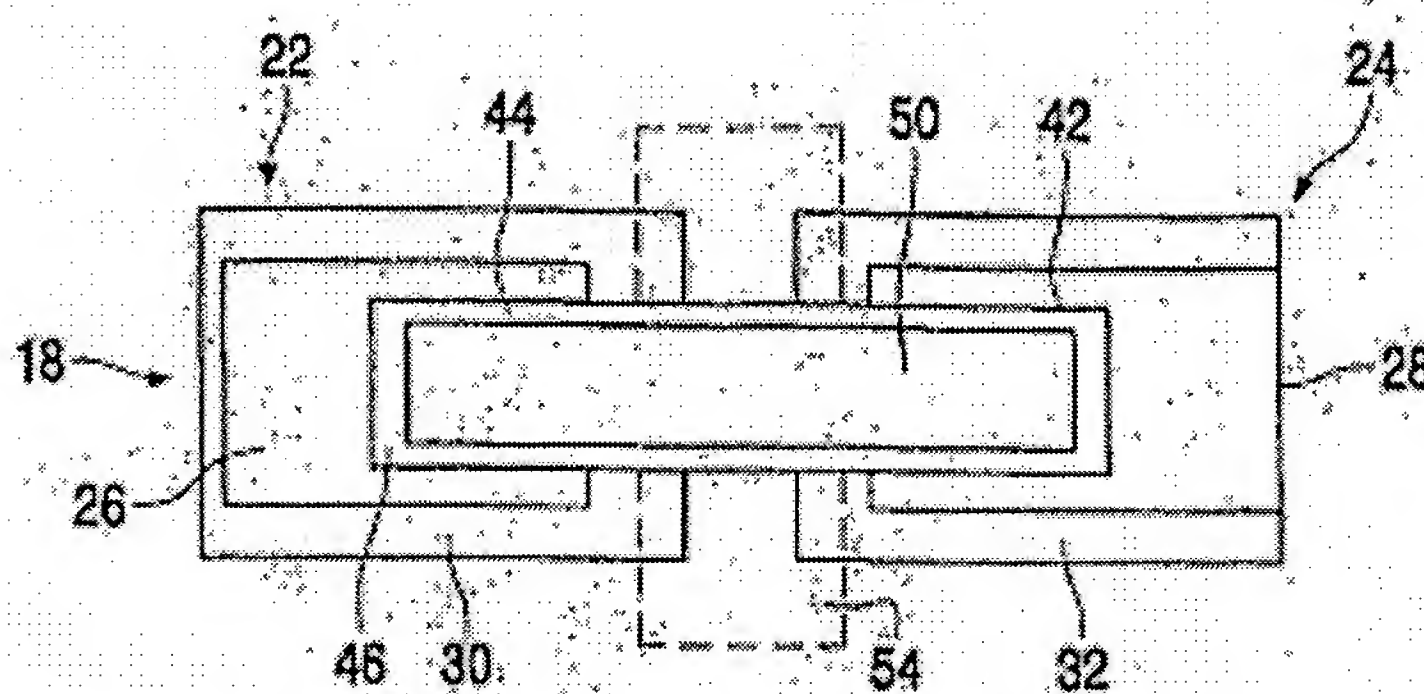


FIG. 3

As shown above and consistent with the description in paragraph 0042 of the instant application, the insulated trench 42 extends into each of the source/drain and respective contact regions (30/22, 32/28). As represented by the dashed lines in FIG. 2, the end walls 46 extend into the respective source/drain regions, as do the side walls 42 as shown in FIG. 3. Referring back to FIG. 48B from the '231 reference, none of the cited portions therein provide correspondence to any trench extending into a source/drain region.

In view of the above, the cited '231 reference does not and cannot correspond to the claimed invention as asserted. As all claim rejections rely upon the erroneous

interpretation and application of the '231 reference as discussed above in connection with independent claim 1, all rejections (including those of dependent claims 2-10) are improper and should be removed.

Applicant further submits that the § 103(a) rejection of claims 1-3 and 5-10 is improper because the Office Action has improperly applied Section 103(a) and any asserted lack of "criticality" of the claimed depths. Specifically, the Office Action fails to present a *prima facie* case of obviousness before Applicant need show the criticality of a claimed range. *See, e.g.*, M.P.E.P. § 2144.05 ("In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976)"). In this instance, the Examiner has not presented a *prima facie* case of obviousness because the Examiner has not cited to any reference that teaches source and drain implantations which have conductive shallow contact regions as discussed above. Moreover, as clearly represented in FIG. 2 of the instant application (copied above) and as well understood in the art, the action of the gate as applied in the trench and respectively with the source and drain regions acts to bias the channel region at depths into the substrate, which can clearly affect the operation of the device. For instance, as represented in FIG. 2, the shown arrows of flow extend down along the sidewall of the gate trench to the lower portion of the buried source/drain regions 30 and 32. Absent this trench and related depth, Applicant notes that the bias applied to the gate would appear to be restricted to an upper portion of the channel region (*e.g.*, as shown by the upper line of lateral arrows in FIG. 2). In this context, the Office Action's assertion that no results are obtained by the claimed invention is not only contrary to Applicant's specification, it is also contrary to well-understood characteristics of semiconductor physics.

Applicant further traverses the § 103(a) rejection of claims 1-3 and 5-10 because the proposed modification of the '231 reference would appear to render it inoperable for its intended purpose (*i.e.*, by widening the trench into the respective source/drain regions, in contrast to FIG. 48B), and because the Office Action has provided no evidence of motivation to modify the '231 reference to include the trench as claimed.

Applicant respectfully traverses the § 103(a) rejection of claim 4 because the cited portions of the '348 reference do not correspond to the claimed invention as discussed

above in relation to the § 103(a) rejection of claim 1, in that the respective potential plate regions (and the trench itself) do not extend into the source/drain regions. Moreover, the alleged motivation is misplaced because the proposed modification would render the '348 reference inoperable as claimed (and referenced above), and further because there is no need for such plate regions where the cited trench does not extend as claimed, as consistent with the copied figures above from the instant application and cited reference. Accordingly, Applicant requests that the § 103(a) rejection of claim 4 be withdrawn.

Applicant has amended claim 1 to correct a formality. New claims 13 and 14 are also believed to be allowable over the cited references for reasons including those indicated above, and further because the cited references fail to disclose limitations directed to a gate trench region "having opposing ends respectively into the source region and the drain region" or to "the dielectric material at each end of the gate trench region being in contact with each of the respective source and drain regions on respective opposing endwalls and sidewalls of the trench." Support for these limitations may be found throughout the specification and figures, with exemplary embodiments shown in FIG. 2, FIG. 3 and corresponding discussion therewith.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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